General Description

The SE8232 is a dimmable constant current LED driver with active power factor correction. It supports high power factor across a wide range of line voltages, and it drives the converter in the Quasi-Resonant (QR) mode to achieve the higher efficiency. By using Primary Side Regulation (PSR), the SE8232 controls the output current accurately without a shunt regulator and an opto-coupler at the secondary side, reducing the external component count, the cost, and the volume of the driver board.

The SE8232 is compatible with the analog dimming. The output current can be modulated by the PWM duty ratio or the average level of DIM pin.

The SE8232 embeds comprehensive protection functions for robust designs, including LED open-circuit protection, LED short-circuit protection, output diode short-circuit protection, VDD Under-Voltage Lockout (UVLO), VDD Over-Voltage Protection (VDD OVP), over load protection, input under / over voltage protection, external / internal Over-Temperature Protection (OTP), and cycle-by-cycle current limitation.

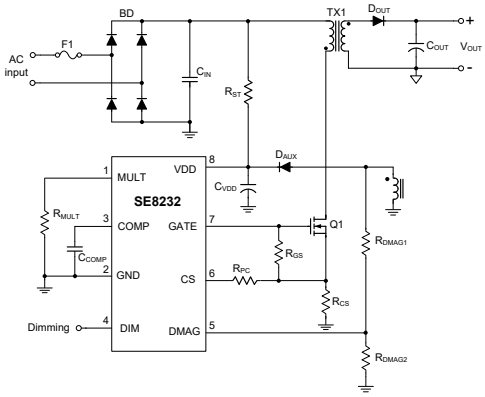
Features

- Tight LED Current Regulation
- Smart CC/CV Mode Control
- Wide Dimming Range (1% to 100%)
- Power Factor Correction
- THD Optimization (THD < 10%)
- Quasi-Resonant (QR) Operation
- Fast Startup
- Adjustable CV level
- Soft Drive for the Better EMI Performance
- Multiple Protection Features
  - LED Open-Circuit Protection
  - LED Short-Circuit Protection
  - Over Load Protection
  - Input Under / Over Voltage Protection
  - Output Diode Short-Circuit Protection
  - VDD Under Voltage Lockout
  - VDD Over Voltage Protection
  - External / Internal OTP
  - Cycle-by-Cycle Current Limitation

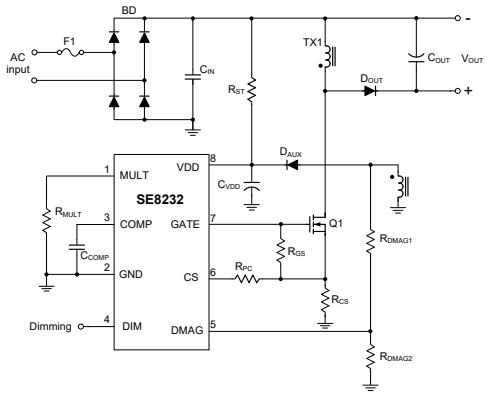
Applications

- AC-DC LED Lighting Driver

Simplified Application Circuit

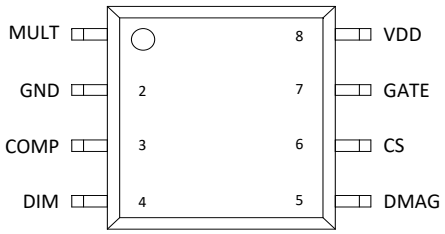


Flyback Application Circuit



Buck-Boost Application Circuit

Pin Configuration



SOP-8

Functional Pin Description

Pin No.	Pin Name	Description
1	MULT	Multi function. Set CV reference voltage and QR delay.
2	GND	Ground of the controller.
3	COMP	Compensation node. Output of the internal trans-conductance amplifier.
4	DIM	Dimming signal input. LED driving current can be modulated by the PWM duty ratio or the average level of this pin.
5	DMAG	Demagnetization pin. To detect the input and the output voltage from the auxiliary winding of the transformer.
6	CS	Current sense input. Connect this pin to the current sense resistor.
7	GATE	Gate driver output for an external power MOSFET.
8	VDD	Supply voltage (V_{DD}) input. The controller will be enabled when V_{DD} exceeds V_{TH_ON} and disabled when V_{DD} is lower than V_{TH_OFF}.

Ordering Information

Device	Package	Temp	Ship Info	Logo
SE8232	SOP-8	-40°C~125°C	Tape 4KPCS/Reel	SE8232XX

Absolute Maximum Ratings(Note 1)

Item	Range
Supply Voltage, VDD	0.3V to 40V
Gate Driver Output, GATE	0.3V to 18V
Other Pins	0.3V to 6.5V
Power Dissipation, P_D @ T_A = 25°C SOP-8	0.48W
Package Thermal Resistance(Note 2) SOP-8, θ_{JA}	206.9°C/W
Lead Temperature (Soldering, 10 sec.)	260°C
Junction Temperature	150°C
Storage Temperature Range	65°C to 150°C
ESD Susceptibility(Note 3) HBM (Human Body Model)	2kV

Recommended Operating Conditions(Note 4)

Item	Range
Supply Input Voltage, VDD	11V to 34V
Junction Temperature Range	-40°C to 125°C

Electrical Characteristics

(V_{DD} = 30V, T_A = 25°C, unless otherwise specified)

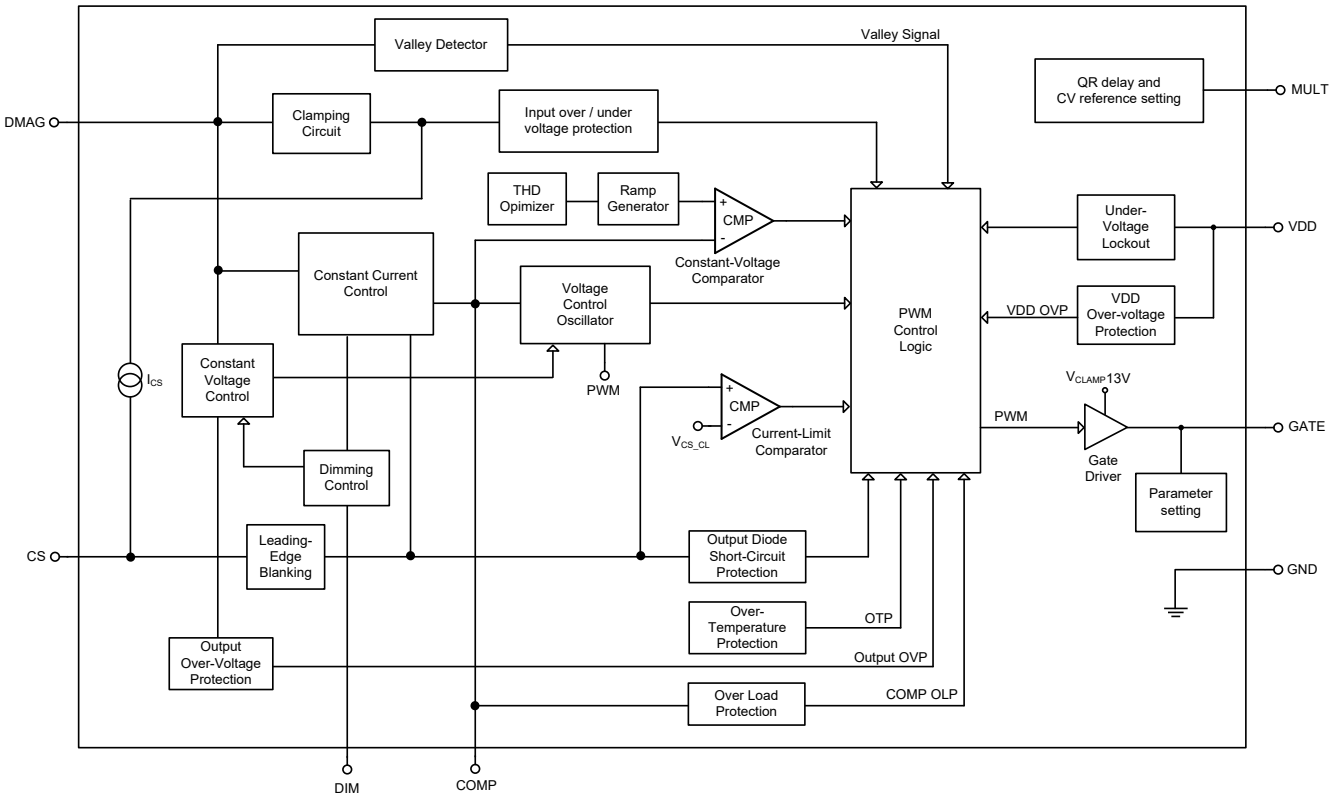
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Section (VDD)						
VDD OVP Threshold Voltage	V_{DD_OVP}		--	37	--	V
Rising UVLO Threshold Voltage	V_{TH_ON}		--	20	--	V
Falling UVLO Threshold Voltage	V_{TH_OFF}		--	9	--	V
VDD Holdup Mode Entry Point	V_{DD_ET}		--	10.4	--	V
VDD Holdup Mode Ending Point	V_{DD_ED}		--	11	--	V
Start-up Current	I_{DD_ST}	$V_{DD} = V_{TH\_ON} - 1V$	--	1.5	--	μA
Operating Current	I_{DD_OP}	V_{DD} = 15V, GATE and COMP pin open	--	900	--	μA
DMAG Section (DMAG)						
Lower Clamp Voltage	V_{DMAG_L}	I_{DMAG} = 1mA	--	100	--	mV
DMAG OVP Threshold Voltage	V_{DMAG_OVP}		--	3.8	--	V
Threshold Current of Brown-in Protection	I_{DMAG_BRI}		--	320	--	μA
Threshold Current of Brown-out Protection	I_{DMAG_BRO}		--	290	--	μA
Threshold Current of Vin Over Voltage Protection	I_{DMAG_OCP}		--	1600	--	μA
High VIN Entry Level	I_{DMAG_HVSW}		--	700	--	μA
DMAG Reference Voltage	V_{DMAG_REF}	CV mode, R_{MULT} = 3.5kΩ	--	1.2	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DMAG Threshold Voltage of Soft Start	V_{DMAG_SS}	When $V_{DMAG} < V_{DMAG\_SS}$, soft start	--	0.5	--	V
DMAG Threshold for Output UVP	V_{TH_UVP}	$V_{TH\_UVP} = V_{DMAG\_SS}$	--	0.5	--	V
Minimum DMAG Masking Time	$t_{BK(MIN)}$	$t_{BK} = 1 + V_{CS\_PK} \times 2$, $V_{CS} = 0V$	--	1	--	µs
Maximum DMAG Masking Time	$t_{BK(MAX)}$	$t_{BK} = 1 + V_{CS\_PK} \times 2$, $V_{CS} = 1.2V$	--	3.4	--	µs
Constant Current Control Section (COMP)						
COMP Over Load Protection Threshold	V_{COMP_OLP}	V_{COMP} rising	--	4.8	--	V
Minimum COMP Voltage	$V_{COMP(MIN)}$		--	0.5	--	V
Maximum Regulated factor for constant-Current Control	$K_{CC(MAX)}$	$V_{DIM} = 3V$, $V_{COMP} = 3V$	--	250	--	mV
Current Sense Section (CS)						
Leading Edge Blanking Time	t_{LEB}		--	250	--	ns
Low Vin Peak Current Limit at Normal Operation	V_{CL_LV}	$I_{DMAG} < 683µA$	--	1.2	--	V
High Vin Peak Current Limit at Normal Operation	V_{CL_HV}	$I_{DMAG} \geq 700µA$	--	1	--	V
Peak Current Limit in VDD Holdup and CV Mode	V_{CL_MIN}	CV mode or $VDD < V_{DD\_ET}$	--	0.2	--	V
Peak Current Shutdown Voltage Threshold	V_{CS_SD}		--	1.7	--	V
Propagation Delay Compensation Factor	K_{PC}	$I_{CS} = K_{PC} \times I_{DMAG}$, $I_{DMAG} = -500µA$	--	0.022	--	A/A
Threshold Voltage for External OTP	V_{OTP_TH}	$V_{DMAG} = 3V$, $V_{CS} = 4/15*V_{DMAG}$	--	0.8	--	V
Gate Driving Section (GATE)						
Rising Time	t_R	$V_{DD} = 15V$, $C_L = 1nF$ (10% to 90%)	--	270	--	ns
Falling Time	t_F	$V_{DD} = 15V$, $C_L = 1nF$ (10% to 90%)	--	40	--	ns
Gate Output Clamping Voltage	V_{CLAMP}	$V_{DD} = 15V$	--	13	--	V
Internal Pull Low Resistor	R_{GATE}	$VDD < V_{TH\_ON}$, before startup	--	40	--	kΩ
Timing Control Section						
Minimum Switching Period	$t_{S(MIN)}$	$V_{COMP} > 2V$	--	8.5	--	µs
Minimum Switching Period in Green Mode	$t_{S(MIN)\_GM}$	$V_{COMP} < 0.5V$	--	500	--	µs
Start Time During Startup and Normal Operation	t_{START}	$V_{COMP} > 2V$	--	127.5	--	µs
Max. Start time in Green Mode	t_{START_GM}	$V_{COMP} < 0.5V$	--	7.5	--	ms
Minimum On Time	$t_{ON(MIN)\_LV}$	$I_{DMAG} = -500µA$	--	800	--	ns
	$t_{ON(MIN)\_HV}$	$I_{DMAG} = -900µA$	--	600	--	ns
Maximum On Time	$t_{ON(MAX)}$		--	20	--	µs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Protection (OTP) Section						
Initial Over Temperature Protection Threshold	T_{OTP_INTH}	FT test 25C Voltage threshold	--	140	--	°C
Over Temperature Protection Threshold After Start-up	T_{OTP_STTH}	FT test 25C Voltage threshold	--	160	--	°C
Dimming Section						
Analog Dimming High Threshold Voltage	V_{DIM_HIGH}		--	2.8	--	V
Analog Dimming Low Threshold Voltage	V_{DIM_LOW}		--	362.5	--	mV
Analog Dimming Enable Threshold Voltage	V_{DIM_EN}		--	300	--	mV
Analog Dimming Disable Threshold Voltage	V_{DIM_DIS}		--	250	--	mV
Parameter Setting Section (MULT)						
Detection Sourcing Current	I_{det}	During t_{det}	--	20	--	µA

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a low effective-thermal-conductivity two-layer test board on a JEDEC thermal measurement standard.
Note 3. 5ŜøłŎŜă ⅠŜ 9{5 ăŜyãłúłøŜ Ⅰ ⅠyŘfłyƎ ǈŜŎⅠdzúłƻyʹłă ŜŎƻYYŜyŘŜŘ
Note 4. The device is not guaranteed to function outside its operating conditions.
Note 5. Guarantee by design.

Functional Block Diagram



Operation

Critical-Conduction Mode (CRM) with Constant On-Time Control

Figure 1 shows a typical flyback converter with the input voltage (V_{IN}). When the main switch Q1 is turned on with a fixed on-time (t_{ON}), the peak current (I_{L_PK}) of the magnetizing inductance (L_m) can be calculated by the following equation:

$$I_{L\_PK} = \frac{V_{IN}}{L_m} \times t_{ON}$$

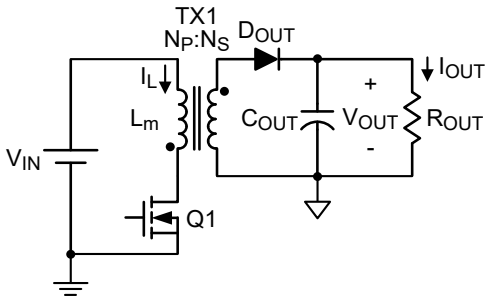


Figure 1. Typical Flyback Converter

If the input voltage is the output voltage of the full-bridge rectifier (V_{IN_PK} x $|\sin\theta|$), the inductor peak current (I_{L_PK}) can be expressed as the following equation:

$$I_{L\_PK} = \frac{V_{IN\_PK} \times |\sin(\theta)| \times t_{ON}}{L_m}$$

As shown in Figure 2, when the converter operates in CRM with the constant on-time control, the envelope of the peak inductor current is in phase with the input voltage. Thus, the high power factor can be achieved.

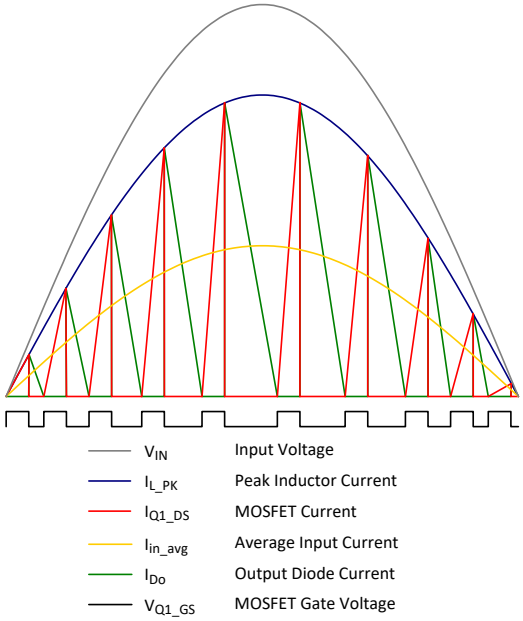


Figure 2. Inductor Current of CRM with Constant On-Time Control

The SE8232 needs no shunt regulator and opto-coupler at the secondary side to achieve the output current regulation. Figure 3 shows several key waveforms of a conventional flyback converter in Quasi-Resonant (QR) mode, in which V_{AUX} is the voltage on the auxiliary winding of the transformer.

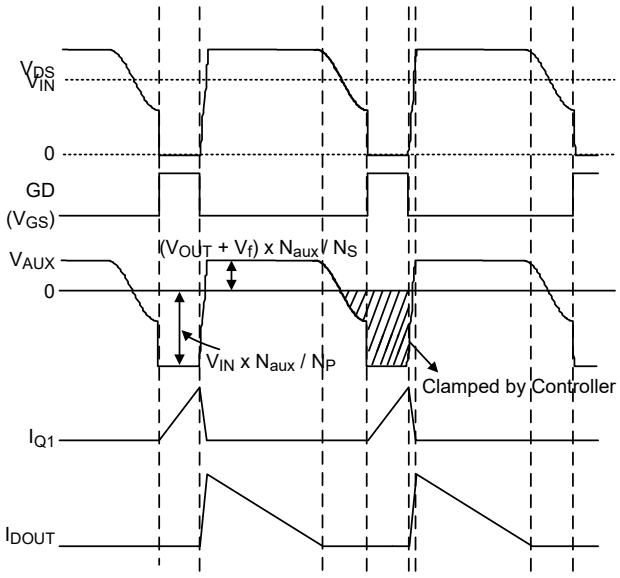


Figure 3. Key Waveforms of a Flyback Converter

Voltage Clamping Circuit

The SE8232 provides a voltage clamping circuit at DMAG pin since the voltage on the auxiliary winding is negative when the main switch is turned on. The lowest voltage on DMAG pin is clamped near zero to prevent the IC from being damaged by the negative voltage. Meanwhile, the sourcing DMAG current (I_{DMAG}), flowing through the

upper resistor (R_{DMAG1}), is sampled and held to be a line-voltage-related signal for propagation delay compensation. The SE8232 embeds the programmable propagation delay compensation through CS pin. A sourcing current I_{CS} (equal to I_{DMAG} x K_{PC}) applies a voltage offset (I_{CS} x R_{PC}) which is proportional to line voltage on CS to compensate the propagation delay effect. Thus, the output current can be equal at high and low line voltage.

Quasi-Resonant Operation

Figure 4 illustrates how valley signal triggers PWM. If no valley signal detected for a long time, the next PWM is triggered by a starter circuit at the end of the interval (t_{START}, 127.5μs typ.). A blanking time ($t_{S(MIN)}$, 8.5μs typ.), which starts at the rising edge of the previous PWM signal, limits minimum switching period. When the $t_{S(MIN)}$ interval is on-going, all of valley signals are not allowed to trigger the next PWM signal. After the end of the $t_{S(MIN)}$ interval, the coming valley will trigger the next PWM signal. If one or more valley signals are detected during the tS(MIN) interval and no valley is detected after the end of the $t_{S(MIN)}$ interval, the next PWM signal will be triggered automatically at the end of the $t_{S(MIN)}$ + 5μs (typ.).

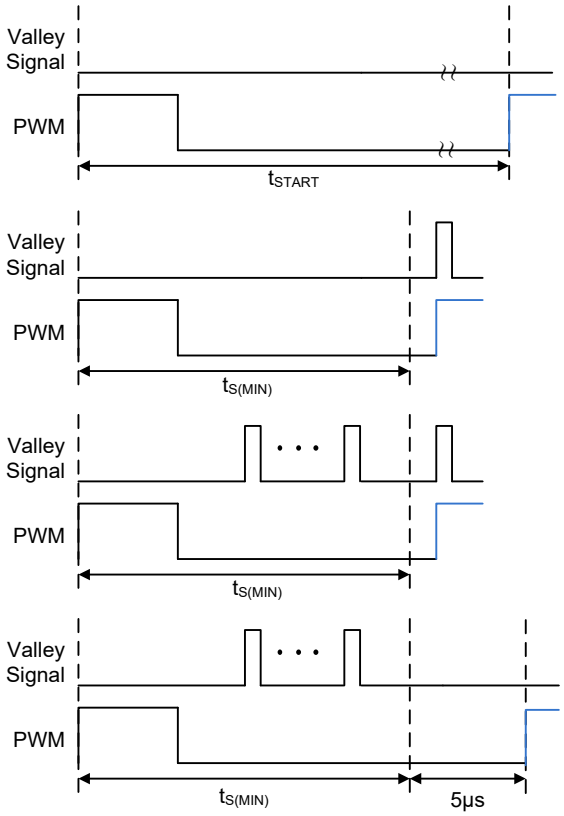


Figure 4. PWM Triggered Method

Dimming Function

The SE8232 features the analog and PWM dimming function. When the average voltage on the DIM pin (V_{DIM}) is within V_{DIM_LOW} and V_{DIM_HIGH}, the regulation factor of the constant current control (K_{CC}) is linearly proportional to V_{DIM}. The suggested PWM high level is 3.3V while the low level is 0V. The frequency of the PWM signal is recommended to be within 500 to 2kHz. The analog and PWM dimming curves are shown in Figure 5. If it is desired to design with non-dim function, a 1MΩ resistor should be connected to VDD pin.

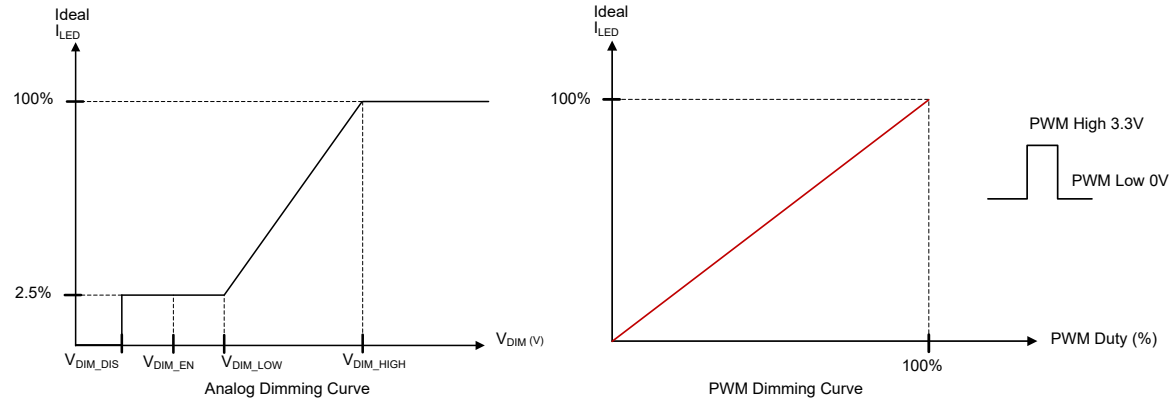


Figure 5. Dimming Curve

CV Mode

When V_{DIM} is lower than V_{DIM_DIS} for 15ms (typ.), the SE8232 will operate in CV mode. The output voltage is regulated by sensing the auxiliary winding voltage. Furthermore, the CV reference voltage can be selected by the MULT pin resistor R_{MULT}.

Protections

LED Open-Circuit Protection

In an event of output open circuit, the converter will be shut down to prevent being damaged, and it will be auto-restarted when the output is recovered. Once the LED is open-circuit, the output voltage keeps rising, causing the voltage on DMAG pin V_{DMAG} rising accordingly. When the sample-and-hold DMAG voltage exceeds its OV threshold (V_{DMAG_OVP}, 3.8V typ.), output OVP will be activated and the GATE will be forced low to turn off the main switch. If the output is still open-circuit when the converter restarts, the converter will be shut down again.

LED Short-Circuit Protection

The SE8232 implements LED short-circuit protection by DMAG and CS pins. Once the DMAG voltage is lower than 0.5V (typ.) and the current sense voltage V_{CS} exceeds the peak current limitation (V_{CS_CL}) for few cycles, the converter will be shut down to prevent damage. It will be auto-restarted when the output is recovered.

The LED short-circuit protection is masked during the first 30ms (typ.) of power on (VDD > V_{TH_ON}).

Output Diode Short-Circuit Protection

When the output diode is damaged as short-circuit, the transformer will be led to magnetic saturation and the main switch will suffer from a high current stress. To avoid the above situation, an output diode short-circuit protection is built-in. When CS voltage V_{CS} exceeds the threshold (V_{CS_SD} 1.7 typ.) of the output diode short-circuit protection, the SE8232 will shut down the PWM output (GATE pin) in few cycles to prevent the converter from damage. It will be auto-restarted when the fault condition is recovered.

VDD Under-Voltage Lockout (UVLO) and Over-Voltage Protection (VDD OVP)

The SE8232 will be enabled when VDD voltage (V_{DD}) exceeds rising UVLO threshold (V_{TH_ON}, 20V typ.) and disabled when V_{DD} is lower than falling UVLO threshold (V_{TH_OFF}, 9V typ.).

When VDD exceeds its over-voltage threshold (V_{DD_OVP}, 37V typ.), the PWM output of the SE8232 is shut down. It will be auto-restarted when the VDD is recovered to a normal level.

In order to ensure the VDD voltage can drop to UVLO threshold to reset some protection function, it is recommended to provide the power for the SE8232 VDD from the auxiliary winding of the transformer.

Input Over-Voltage and Under-Voltage Protection

When I_{DMAG} is over the threshold current of V_{IN} over-voltage protection (I_{DMAG_OCP}) in few cycles, the GATE will shut down to avoid over stress on components. As soon as the input voltage drops below the brown-out threshold for 70ms (typ.), the controller will shut down until it recovers to the brown-in threshold.

Over Load Protection

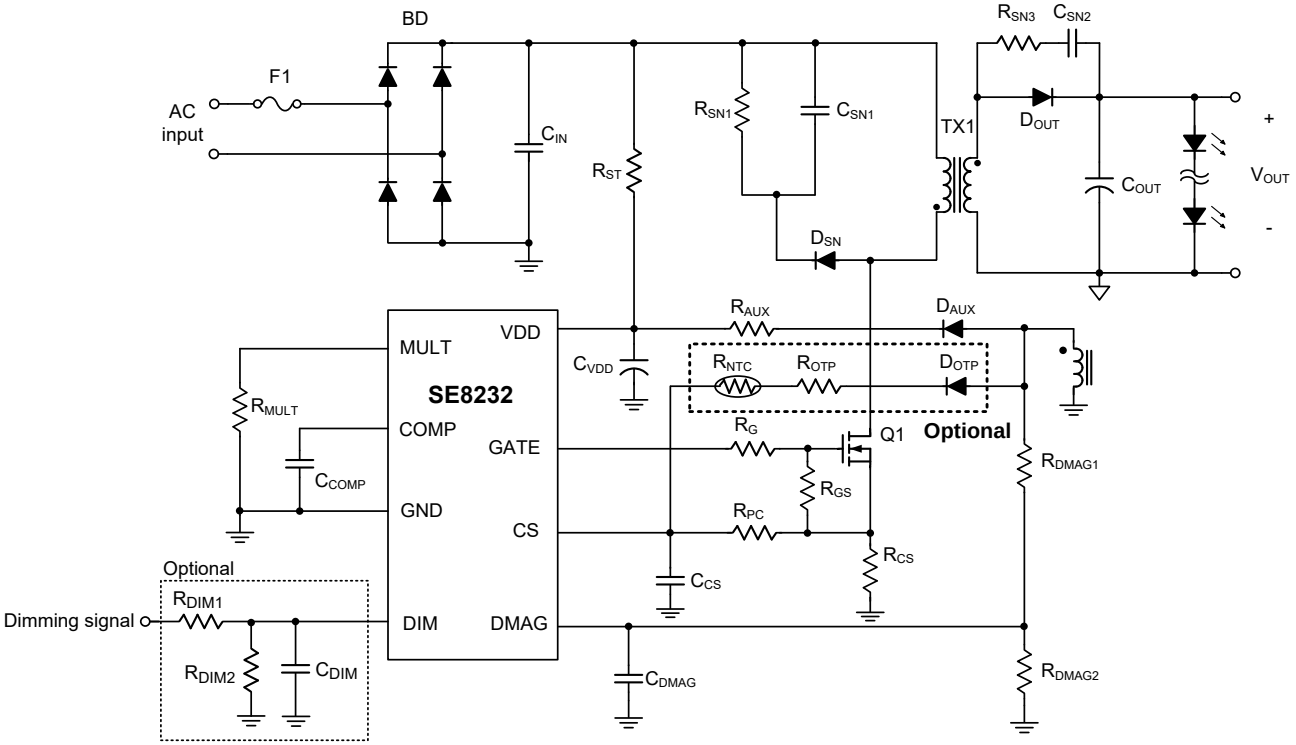
If the current sense resistor R_{CS} is short-circuit, the COMP voltage will increase and result in over load operation. When V_{COMP} reaches to V_{COMP_OLP} (4.8V typ.) for 70ms (typ.), the main switch will be turned off.

Internal and External Over-Temperature Protection (OTP)

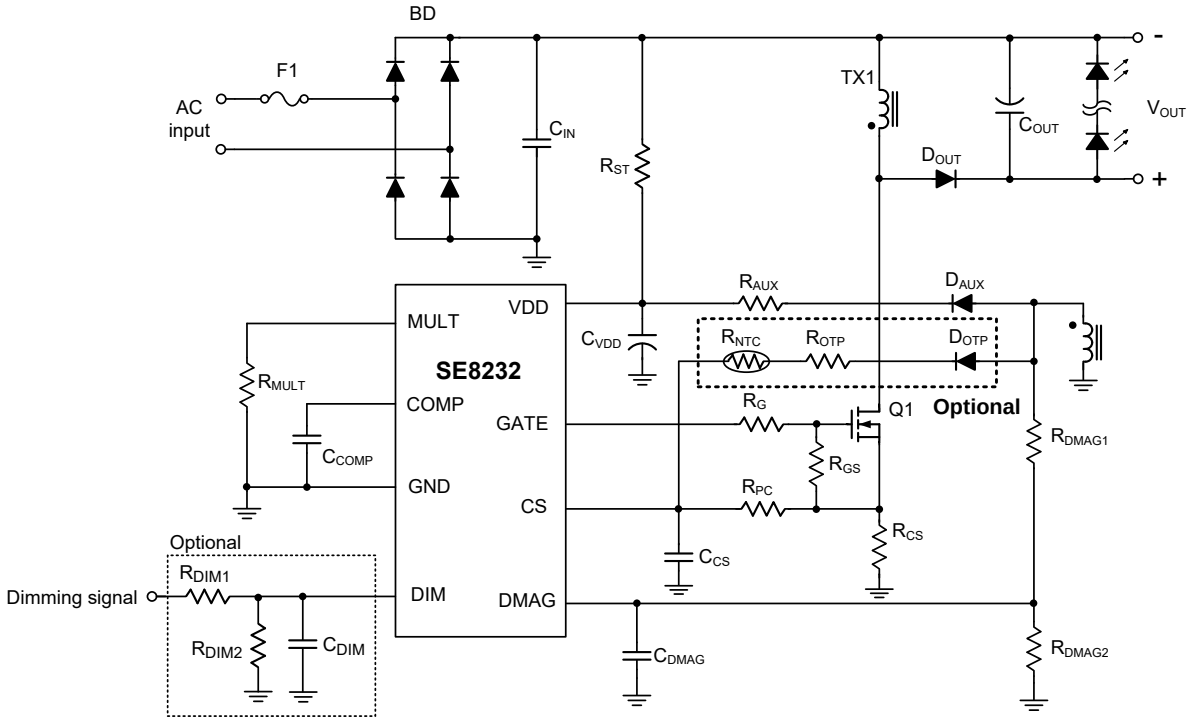
The SE8232 provides the internal OTP function to protect the controller itself from suffering the thermal stress and permanent damage. Once the junction temperature is higher than the OTP threshold (T_{OTP_STTH}, 160°C typ.), the controller will shut down until the temperature decreases below 140°C (typ.). The external OTP function is achieved by the CS pin. If the CS voltage V_{CS}, which is during the turn-off period of the main switch, exceeds the external OTP threshold (V_{OTP_TH}) for 70ms (typ.), the controller will shut down until the fault released.

Typical Application Circuit

Flyback Application Circuit

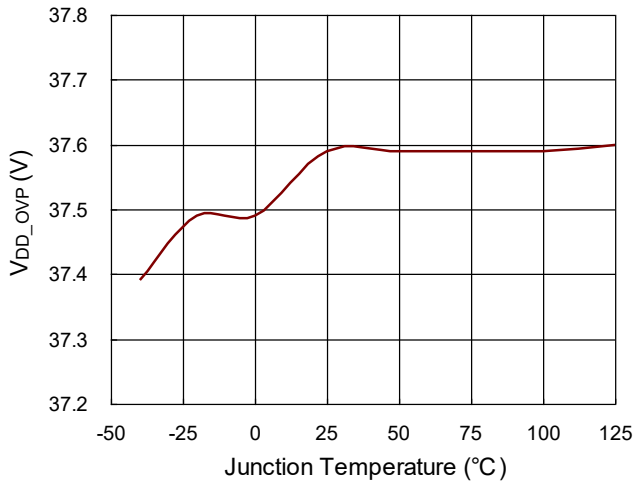


Buck-Boost Application Circuit

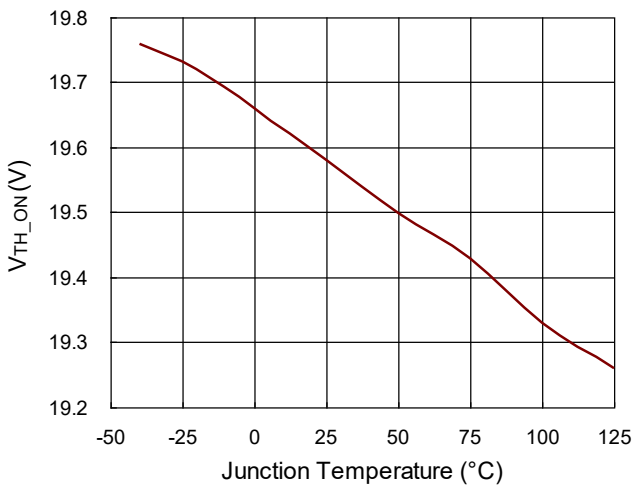


Typical Operating Characteristics

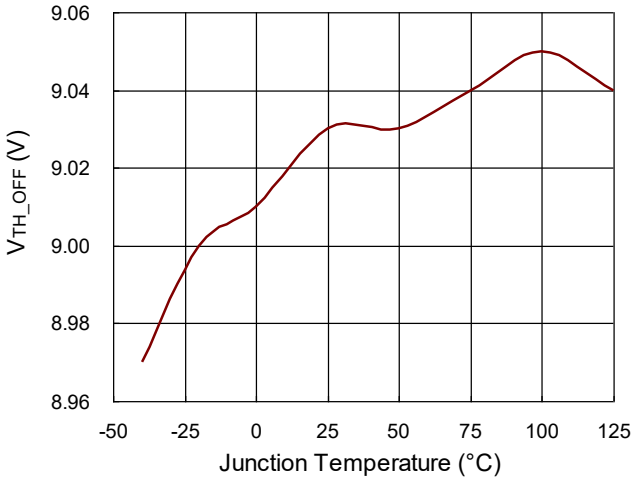
V_{DD_OVP} vs. Junction Temperature



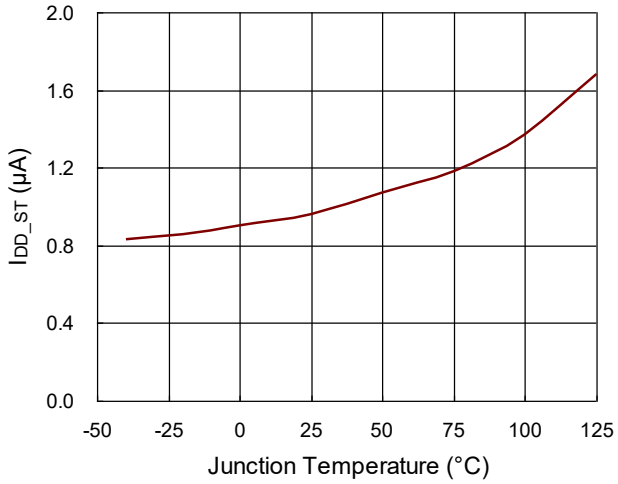
V_{TH_ON} vs. Junction Temperature



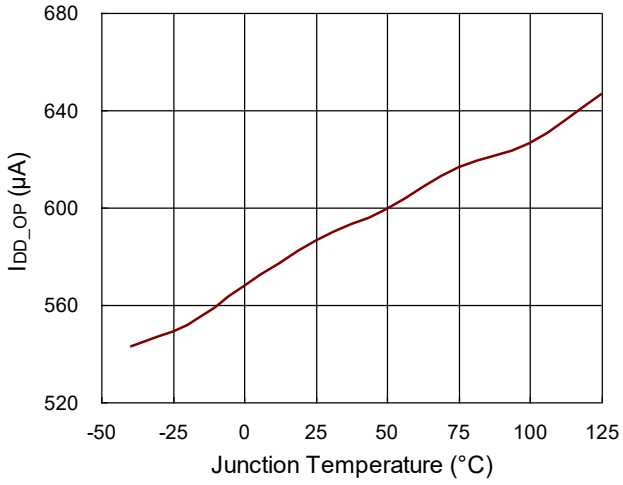
V_{TH_OFF} vs. Junction Temperature



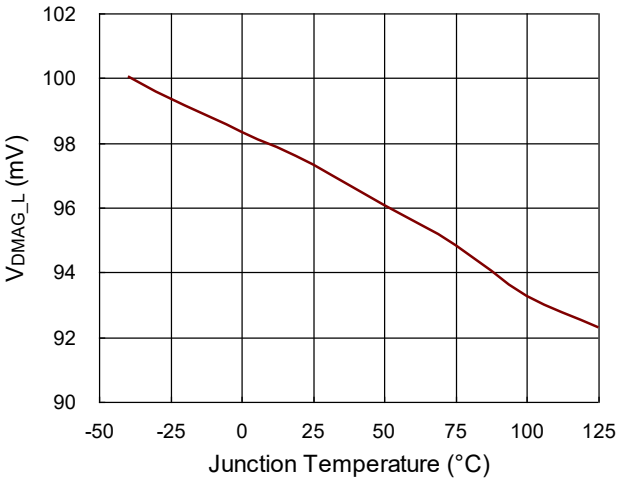
I_{DD_ST} vs. Junction Temperature



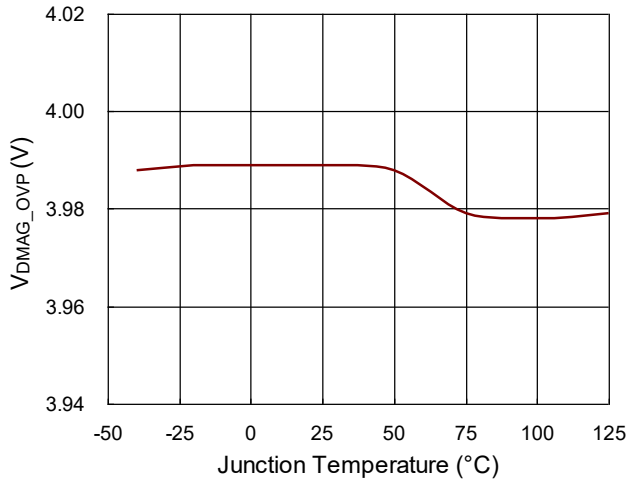
I_{DD_OP} vs. Junction Temperature



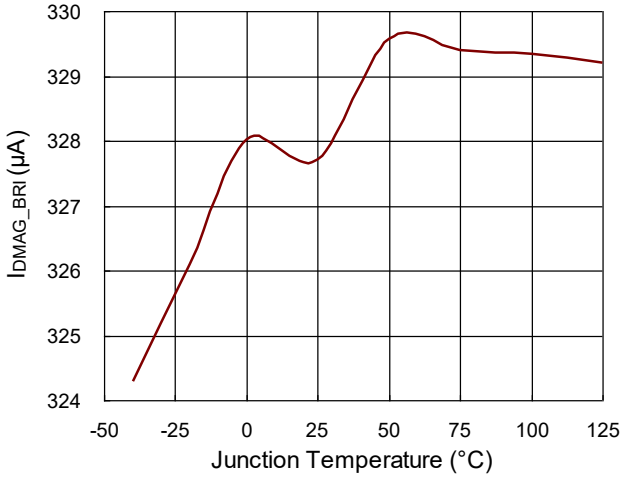
V_{DMAG_L} vs. Junction Temperature



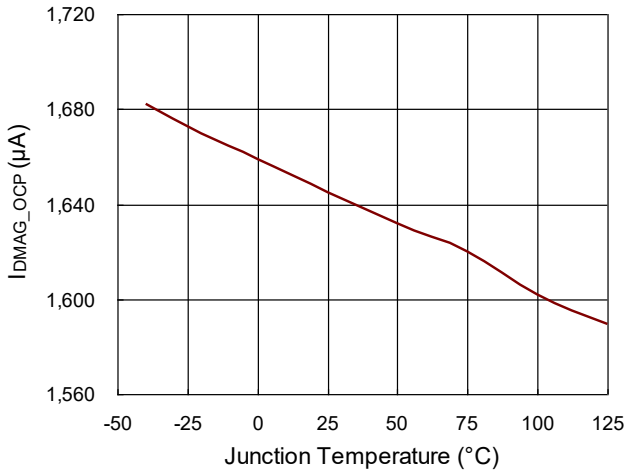
V_{DMAG_OVP} vs. Junction Temperature



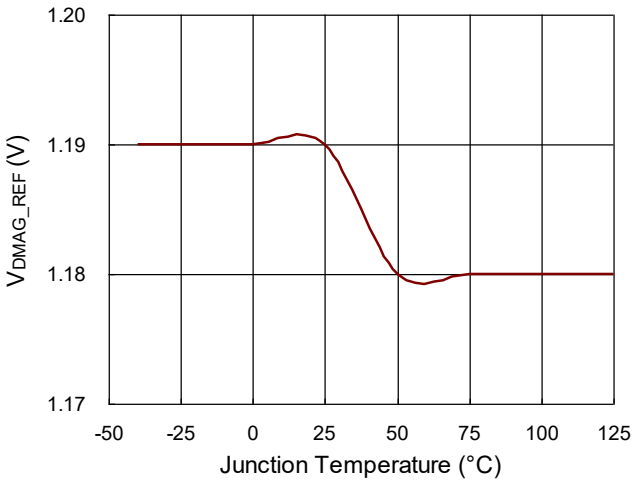
I_{DMAG_BRI} vs. Junction Temperature



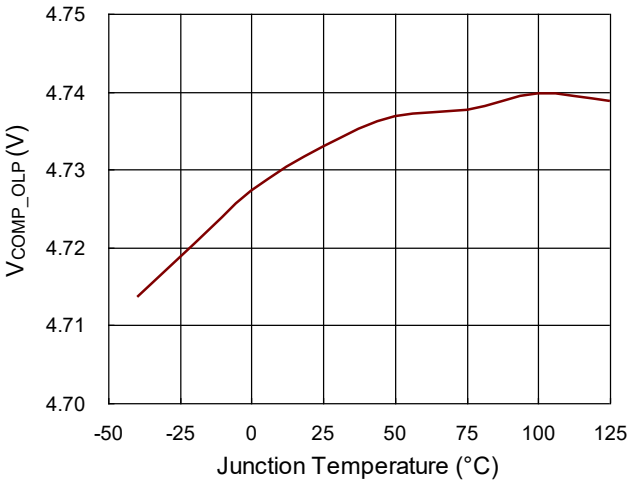
I_{DMAG_OCP} vs. Junction Temperature



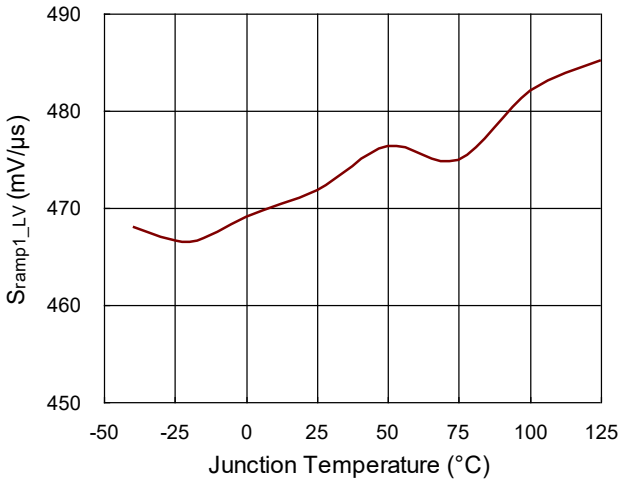
V_{DMAG_REF} vs. Junction Temperature



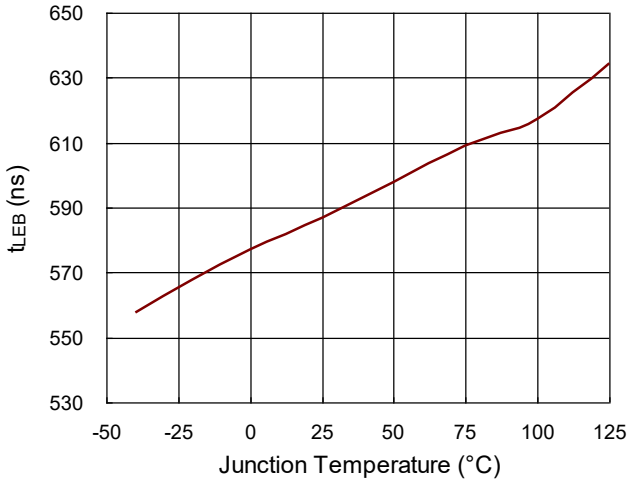
V_{COMP_OLP} vs. Junction Temperature



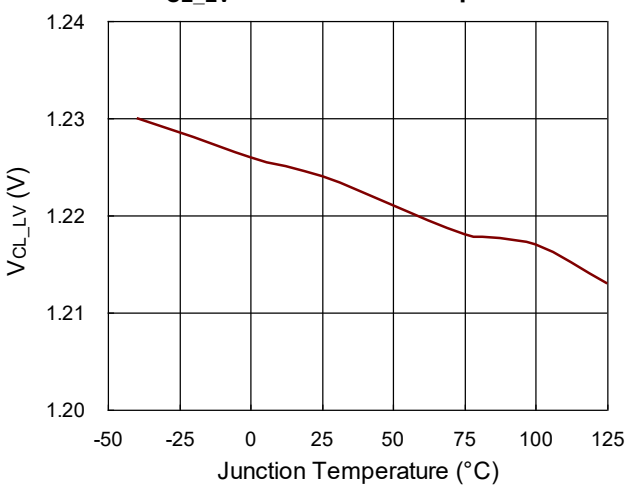
S_{ramp1_LV} vs. Junction Temperature



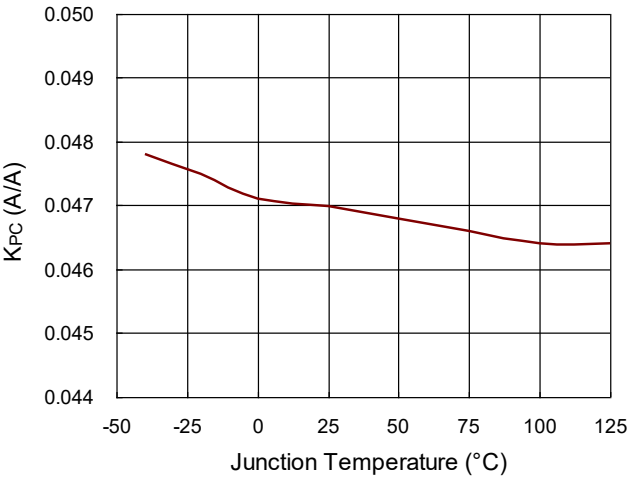
t_{LEB} vs. Junction Temperature



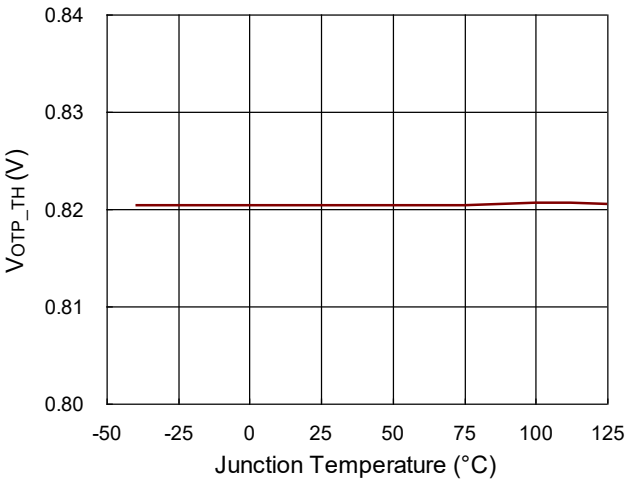
V_{CL_LV} vs. Junction Temperature



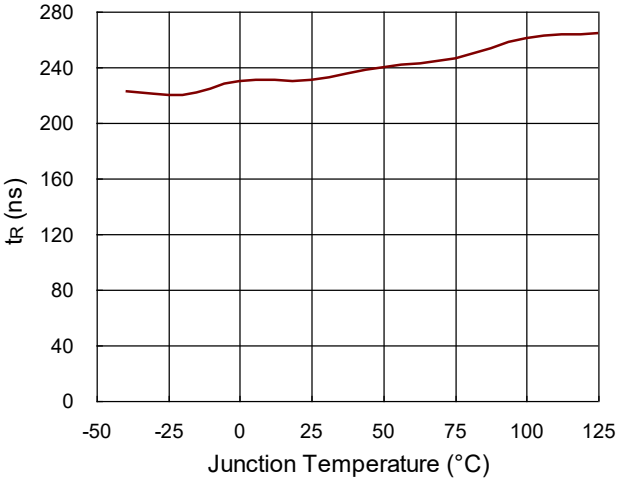
K_{PC} vs. Junction Temperature



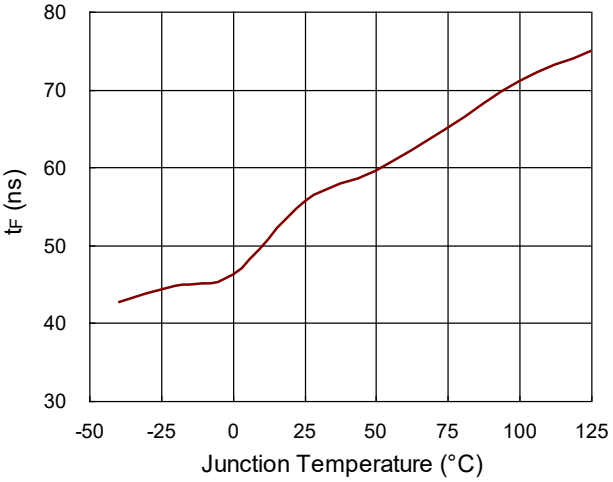
V_{OTP_TH} vs. Junction Temperature



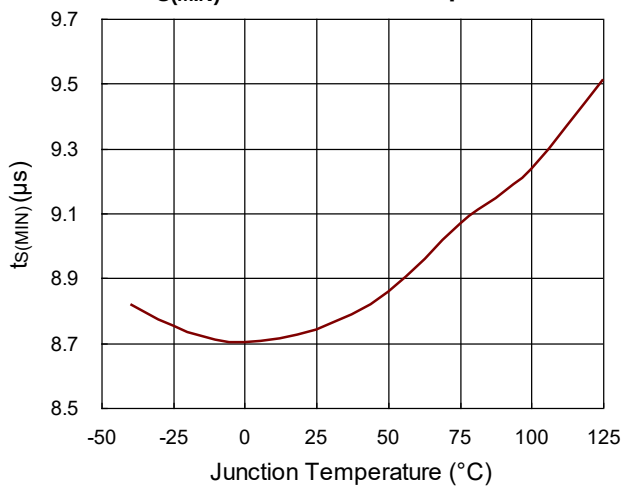
t_R vs. Junction Temperature



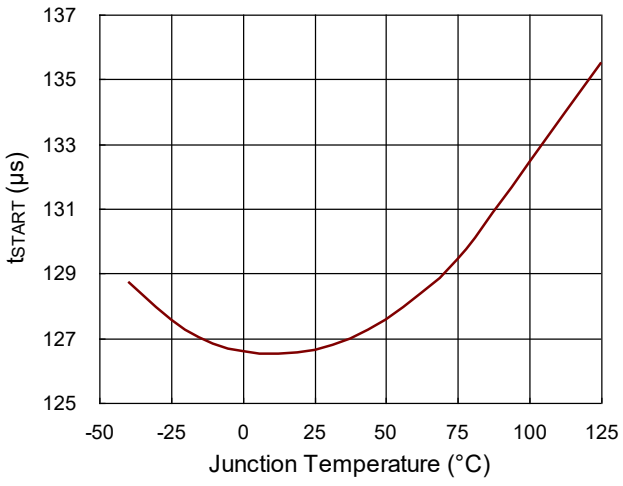
t_F vs. Junction Temperature



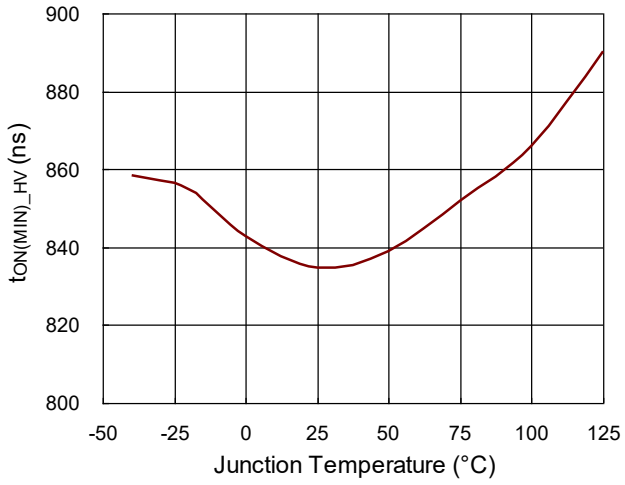
$t_{S(MIN)}$ vs. Junction Temperature



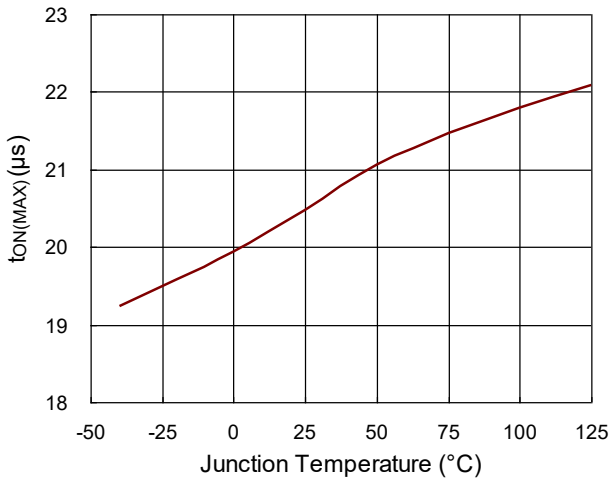
t_{START} vs. Junction Temperature



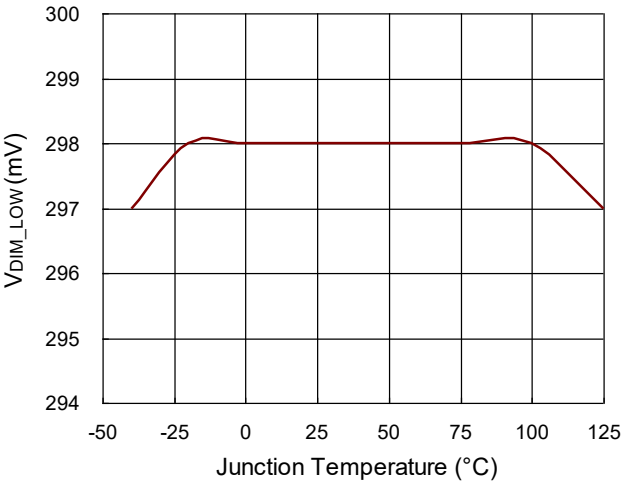
$t_{ON(MIN)\_HV}$ vs. Junction Temperature



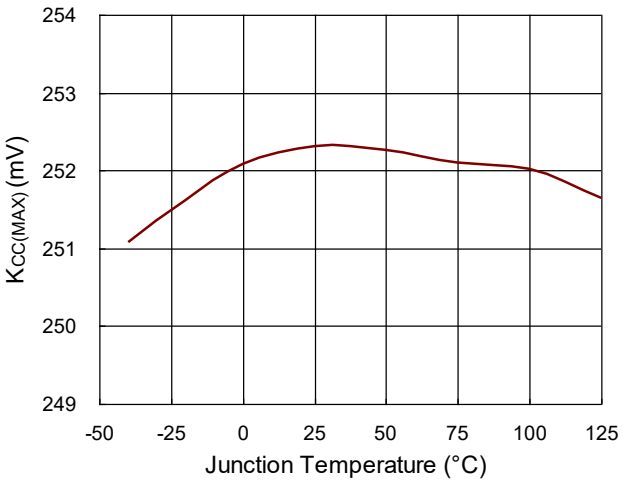
$t_{ON(MAX)}$ vs. Junction Temperature

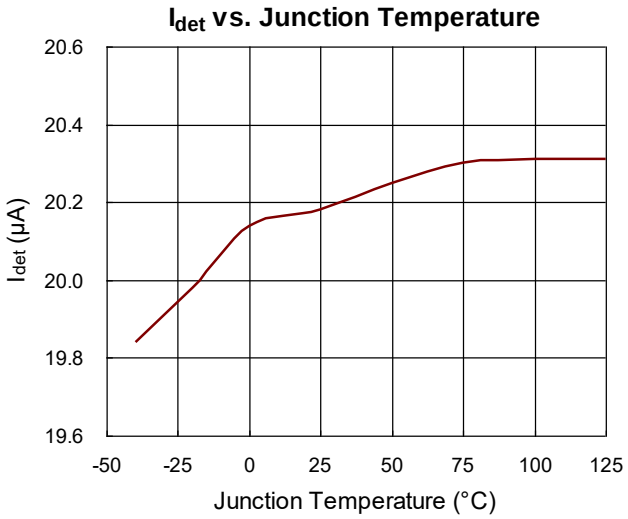


V_{DIM_LOW} vs. Junction Temperature



$K_{CC(MAX)}$ vs. Junction Temperature




I_{det} vs. Junction Temperature
20.6
20.4
20.2
20.0
19.8
19.6
I_{det} (μA)
-50
-25
0
25
50
75
100
125
Junction Temperature (°C)

Application Information

Output Current Setting

Considering the conversion efficiency, the programmed DC level of the average output current ($I_{OUT}(t)$) can be derived as:

$$I_{OUT\_CC} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{R_{CS}} \times CTR_{TX1}$$

$$CTR_{TX1} = \frac{I_{SEC\_PK}}{I_{PRI\_PK}} \times \frac{N_S}{N_P}$$

in which CTR_{TX1} is the current transfer ratio of the transformer TX1, I_{SEC_PK} is the peak current of the secondary side, and I_{PRI_PK} is the peak current of the primary side. CTR_{TX1} can be estimated to be 0.9. According to the above parameters, current sense resistor R_{CS} can be determined as the following equation:

$$R_{CS} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{K_{CC}}{I_{OUT\_CC}} \times CTR_{TX1}$$

Propagation Delay Compensation Design

The V_{CS} deviation (ΔV_{CS}) caused by propagation delay effect can be derived as:

$$\Delta V_{CS} = \frac{V_{IN} \cdot t_D \cdot R_{CS}}{L_m},$$

in which t_D is the delay period which includes the propagation delay of the SE8232 and the turn-off transition of the main MOSFET. The sourcing current from CS pin of the SE8232 (I_{CS}) can be expressed as:

$$I_{CS} = K_{PC} \cdot V_{IN} \cdot \frac{N_A}{N_P} \cdot \frac{1}{R_{DMAG1}}$$

where N_A is the turns number of the auxiliary winding. R_{PC} can be designed by:

$$R_{PC} = \frac{\Delta V_{CS}}{I_{CS}} = \frac{t_D \cdot R_{CS} \cdot R_{DMAG1}}{L_m \cdot K_{PC}} \cdot \frac{N_P}{N_A}$$

CV Reference and QR Delay Setting

After startup, the CV reference voltage and the QR delay is determined by the MULT pin resistor R_{MULT}. The corresponding values of the different R_{MULT} are as follows:

CV Voltage	QR delay = 100ns to 500ns
1.2V	R_{MULT} = 3.5kΩ to 17.5kΩ
1V	R_{MULT} = 24.5kΩ to 122.5kΩ
0.7V	R_{MULT} = 171.5kΩ to 857.5kΩ

Provided that the CV reference voltage is chosen as 1.2V (typ.) and the estimated half of the resonant period of the magnetizing inductance L_m and the parasitic capacitance of MOSFET is 100ns, R_{MULT} can be designed as the following equation:

$$R_{MULT} = 3.5k\Omega \times \frac{100ns}{100ns} = 3.5k\Omega \ (typ.)$$

COMP Voltage Design

The COMP voltage, V_{COMP}, can be expressed as follows:

$$V_{COMP} = \frac{V_{THDO} \times G_{m\_ramp} \times t_{on\_pk}^2 \times f_{s\_pk}}{C_{ramp}} + V_D$$

where t_{on_pk} and f_{s_pk} are the peak values at V_{IN_PK}, G_{m_ramp} and C_{ramp} are the fixed parameters in SE8232 and the typical values are : G_{m_ramp} = 2.7μA/V, Cramp = 6.5pF. V_D is the offset of the constant-voltage comparator and its typical value is 2V.

V_{THDO} is the input voltage of the THD optimizer and it can be selected as different voltages by the external Gate-to-Source resistor R_{GS}. The recommended R_{GS} is 22kΩ or 47kΩ, and the corresponding values of V_{THDO} are 1.2V (typ.) and 0.9V (typ.), respectively. It is recommended to design V_{COMP} = 3.5 to 4.2V. If V_{COMP} is over 4.2V, the output current regulation may be affected.

Input Under-Voltage Protection Setting

The input voltage is detected by R_{DMAG1}, which is used to set the input UV level (VIN_UVP). Thus, R_{DMAG1} can be determined by the following equation:

$$R_{DMAG1} = V_{IN\_pk} \times \frac{N_A}{N_P} \times \frac{1}{I_{DMAG\_BRI}}$$

where I_{DMAG_BRI} is the fixed parameters in SE8232 and its typical value is 320μA.

Output Over-Voltage Protection Setting

Output OVP is achieved by sensing the voltage on the auxiliary winding. It is recommended that output OV level (V_{OUT_OVP}) is set at 120% of nominal output voltage (V_{OUT}). Thus, R_{DMAG1} and R_{DMAG2} can be determined by the equation as:

$$V_{OUT} \times \frac{N_A}{N_S} \times \frac{R_{DMAG2}}{R_{DMAG1} + R_{DMAG2}} \times 120\% = 3.8V(typ.)$$

Adaptive Blanking Time

When the MOSFET is turned off, the leakage inductance of the transformer and parasitic capacitance (C_{OSS}) of the MOSFET induce resonance waveform on the DMAG pin. The resonance waveform may make the controller false trigger the DMAG OVP, and it may cause the controller operate in unstable condition. As load increases, the resonance time also increases. It is recommended to add a 10pF to 47pF bypass capacitor, and it should be as close to DMAG pin as possible. The larger bypass capacitor may cause phase shift on DMAG waveform, so the MOSFET is not turned on at exact valley point.

To avoid the above issue, the SE8232 provides adaptive blanking time (t_{BK}). It varies with the peak voltage of the CS pin (V_{CS_PK}), as shown by the following formula:

$$t_{BK} = 1\mu s + V_{CS\_PK} \times 2\mu s/V \text{ (typ.)}$$

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a SOP-8 package, the thermal resistance, θ_{JA}, is 206.9°C/W on a standard JEDEC low effective-thermal-conductivity two-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

$P_{D(MAX)}$ = (125°C - 25°C) / (206.9°C/W) = 0.48W for a SOP-8 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

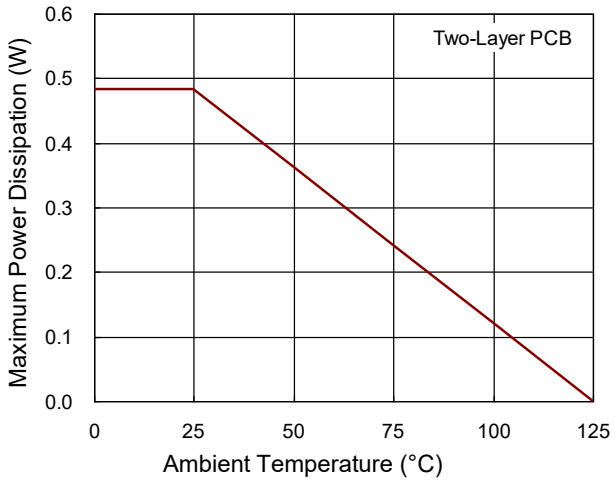


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Considerations

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Please refer to the guidelines when designing a PCB layout for switching power supply :

- The current path(1) from the input capacitor, transformer, MOSFET, R_{CS} returning to input capacitor is a high frequency current loop. The path(2) from GATE pin, MOSFET, R_{CS} returning to the ground of the IC is also a high frequency current loop. They must be as short as possible to decrease noise coupling and kept a space to other low voltage traces, such as IC control circuit paths, especially. Besides, the path(3) between MOSFET ground(b) and IC ground(d) is recommended to be as short as possible, too.
- The path(4) from RCD snubber circuit to MOSFET is a high switching loop. Keep it as small as possible.
- The path(5) from the input capacitor to VDD pin is a high voltage loop. Keep a space from path(5) to other low voltage traces.
- It is good for reducing noise, output ripple and EMI issue to separate ground traces of the input capacitor(a), MOSFET(b), auxiliary winding(c) and IC control circuit(d). Finally, connect them together at the input capacitor ground(a). The areas of these ground traces should be kept large.
- To reduce the parasitic trace inductance and EMI, the area of the loop connecting to the secondary winding, the output diode, and the output filter capacitor must be minimized. In addition, the sufficient copper area at the anode and cathode terminal of the output diode can help for heat-sinking. It is recommended to apply the larger area at the quiescent cathode terminal. The large anode area will induce high-frequency radiated EMI.

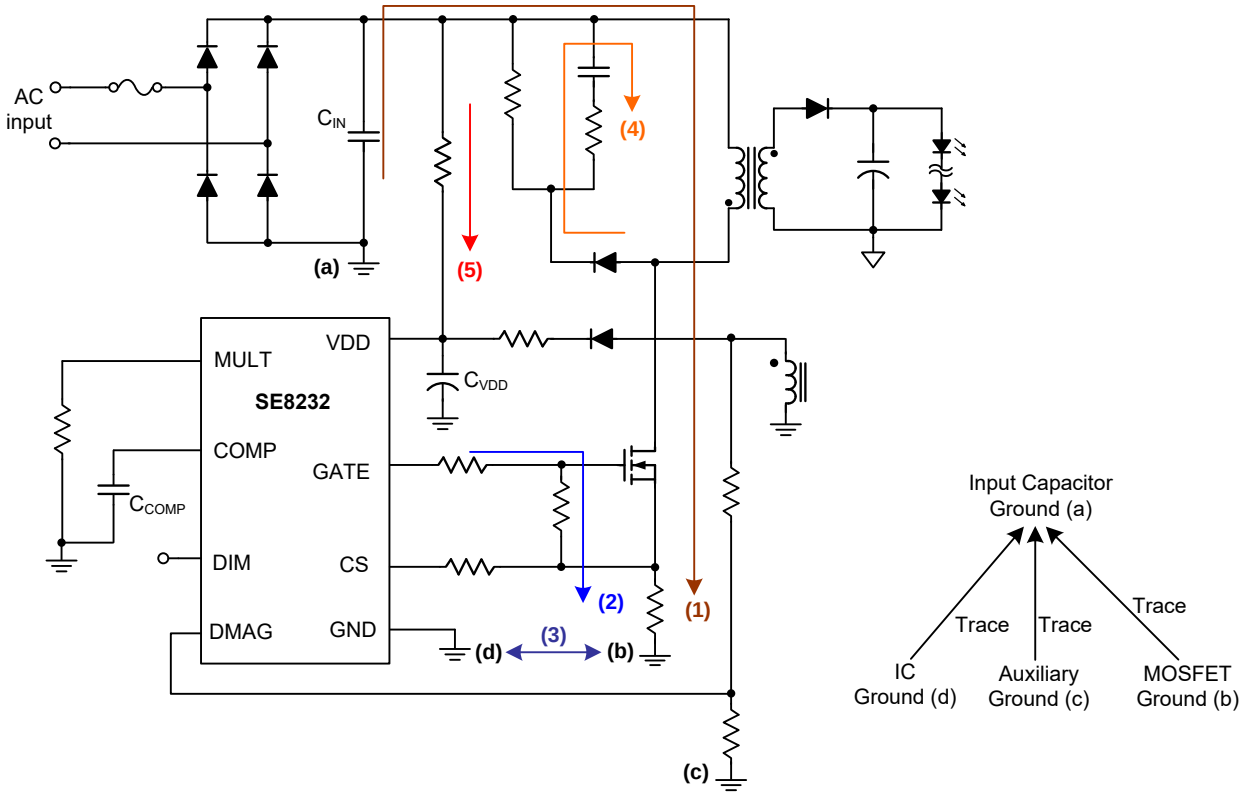
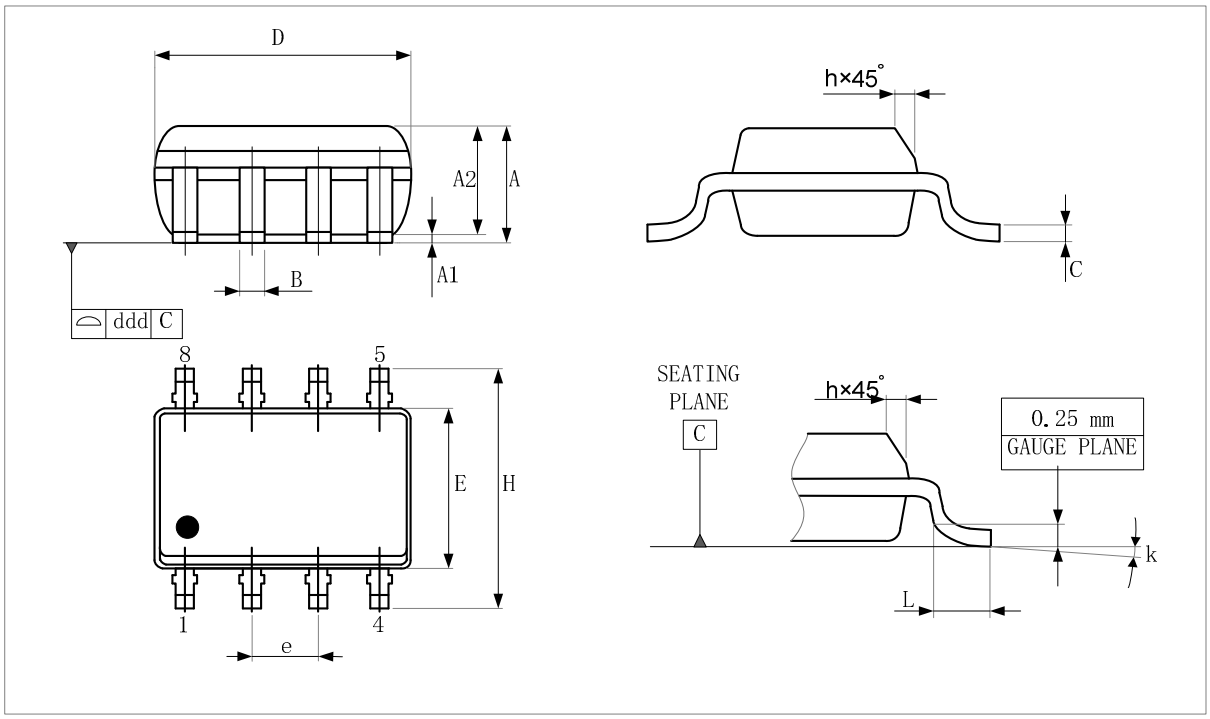


Figure 7. PCB Layout Guide

Package Information

SOP-8



Dim	Data Book (mm)		
	Min	Nom	Max
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	8°(max)		
ddd			0.1